

## **CLAIMS**

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (Previously Presented) A packaged semiconductor device, comprising:

a semiconductor die;

a substrate with the semiconductor die disposed therein;

a plurality of leads coupled to the semiconductor die, wherein at least one said lead has a shaped end proximate the substrate and configured to minimize parasitic capacitance over a predetermined frequency range;

an encapsulant enclosing the semiconductor die and plurality of leads, the encapsulant having a constant dielectric constant over the predetermined frequency range; and

the encapsulant operable to shunt thermal capacitance and thermal resistance away from the semiconductor die.

Claim 2 (Original) The packaged semiconductor device as recited in Claim 1, further comprising an I/O common terminal, at least one input terminal and at least one output terminal, coupled to the semiconductor die.

Claim 3 (Original) The packaged semiconductor device as recited in Claim 2, wherein the input terminal(s) and output terminal(s) are positioned orthogonal to the I/O common terminal.

Claim 4 (Original) The packaged semiconductor device as recited in Claim 3, wherein the semiconductor die is positioned above the I/O common terminal.

Claim 5 (Original) The packaged semiconductor device as recited in Claim 4, wherein the encapsulant forms a substantially hexagonal structure surrounding the I/O common terminal, input terminal(s), and output terminal(s), essentially at right angles with respect to the substrate.

Claim 6 (Original) The packaged semiconductor device as recited in Claim 5, further comprising a lead-frame for coupling the input terminal(s) to a circuit and the output terminal(s) to a circuit.

Claim 7 (Original) The packaged semiconductor device as recited in Claim 6, wherein the portion of the lead-frame coupled to each of the input terminal(s) and output terminal(s) possess exposed dovetailed side edges operable to allow epoxy to lock on the sides and top of the exposed edges.

Claim 8 (Original) The packaged semiconductor device as recited in Claim 3, further comprising an end surface of the input terminal(s) being positioned adjacent and parallel to the side surface of the I/O common terminal, and an end surface of the output terminal(s) being positioned adjacent and parallel to the opposing side surface of the I/O common terminal, said end surfaces being shaped so as to minimize parasitic capacitance.

Claim 9 (Previously Presented) The packaged semiconductor device as recited in Claim 1, wherein the configured lead has a rounded shape expanding outward toward the substrate.

Claim 10 (Currently amended) The packaged semiconductor device as recited in Claim 8, further comprising length and width dimensions of approximately .079 millimeters and ~~[[.065]]~~ 0.050 millimeters, respectively, and a height dimension of approximately .032 millimeters.

Claim 11 (Original) The packaged semiconductor device as recited in Claim 8, further comprising an operating frequency range from DC to 10 gigahertz.

Claim 12 (Original) The packaged semiconductor device as recited in Claim 8, further comprising use in a surface mount assembly.

Claim 13 (Original) The packaged semiconductor device as recited in Claim 8, further comprising use in an integrated circuit.

Claim 14. (Original) The packaged semiconductor device as recited in Claim 8, further comprising use in an amplifier gain stages.

Claim 15 (Original) The packaged semiconductor device as recited in Claim 8, further comprising metallization, including a first and second metallization strip, as the means of coupling the input terminal(s) and the output terminal(s) to the semiconductor die.

Claim 16 (Original) The packaged semiconductor device as recited in Claim 15, further comprising a path length from input terminal to the output terminal, of a fraction of the wavelength for which frequency the semiconductor device is designed.

Claim 17 (Original) The packaged semiconductor device as recited in Claim 8, further comprising bond wires as the means of coupling the input terminal(s) and the output terminal(s) to the semiconductor die, the input terminal being coupled to a first end of a first bond wire, a second end of the first bond wire being coupled to the semiconductor die, a first end of a second bond wire being coupled to the semiconductor die, a second end of the second bond wire being coupled to the output terminal.

Claim 18 (Original) The packaged semiconductor device as recited in Claim 17, further comprising a path length from the input terminal to the output terminal of a fraction of the wavelength for which frequency the semiconductor device is designed.

Claim 19 Canceled

Claim 20 (Original) The packaged semiconductor device as recited in Claim 1, further comprising a light emitting semiconductor as the semiconductor die.

Claim 21 (Original) The packaged semiconductor device as recited in Claim 20, further comprising a light emitting diode as the light emitting semiconductor.

Claim 22 (Original) The packaged semiconductor device as recited in Claim 20, further comprising a substantially clear epoxy material as the encapsulant.

Claim 23 (Original) The packaged semiconductor device as recited in Claim 20, further comprising a cathode and an anode as the plurality of leads.

Claim 24 (Original) The packaged semiconductor device as recited in Claim 23, further comprising the positioning of the cathode and the anode opposite to each other.

Claim 25 (Original) The packaged semiconductor device as recited in Claim 24, further comprising an encapsulant with a substantially hexagonal structure around the cathode and the anode essentially at right angles with respect to the substrate.

Claim 26 (Original) The packaged semiconductor device as recited in Claim 23, further comprising a portion of a conductive lead-frame as the cathode.

Claim 27 (Original) The packaged semiconductor device as recited in Claim 23, further comprising a shaped end surface of the cathode operable to minimize parasitic capacitance.

Claim 28 (Original) The packaged semiconductor device as recited in Claim 27, further comprising a rounded shape on the end surface of the cathode.

Claim 29 (Original) The packaged semiconductor device as recited in Claim 23, further comprising metallization as the cathode coupling means to the semiconductor die.

Claim 30 (Original) The packaged semiconductor device as recited in Claim 23, further comprising a bond wire as the means of coupling the cathode to the semiconductor die, a first end of the bond wire being coupled to the cathode and a second end of the bond wire being coupled to the semiconductor die.

Claim 31 (Original) The packaged semiconductor device as recited in Claim 23, further comprising a portion of a conductive lead-frame as the anode.

Claim 32 (Original) The packaged semiconductor device as recited in Claim 23, further comprising a shaped end surface of the anode operable to minimize parasitic capacitance.

Claim 33 (Original) The packaged semiconductor device as recited in Claim 32, further comprising a rounded shape on the end surface of the anode.

Claim 34 (Original) The packaged semiconductor device as recited in Claim 23, further comprising metallization as the anode coupling means to the semiconductor die.

Claim 35 (Original) The packaged semiconductor device as recited in Claim 23, further comprising a bond wire as the means of coupling the anode to the semiconductor die, a first end of the bond wire being coupled to the anode and a second end of the bond wire being coupled to the semiconductor die.

Claim 36 Canceled

Claim 37 (Original) The packaged semiconductor device as recited in Claim 20, further comprising being adapted for use in an integrated circuit.

Claim 38 (Original) The packaged semiconductor device as recited in Claim 20, further comprising being adapted for use in a surface mount assembly.

Claim 39 (Previously Presented) The packaged semiconductor device as recited in Claim 20, having length and width dimensions of approximately .079 millimeters and .050 millimeters, respectively, and a height dimension of approximately .032 millimeters.

Claim 40 (Currently amended) A packaged semiconductor device, comprising:  
a light emitting semiconductor, a substrate, a terminal, and an encapsulant material;  
the light emitting semiconductor being disposed in the substrate;  
a means coupling the terminal to the light emitting semiconductor;  
the **terminal further comprising a** terminal shaped end configured to minimize parasite capacitance over a predetermined frequency range;  
a substantially clear encapsulant for encapsulating the light emitting semiconductor, the encapsulant material acting as a thermal shunt to ground operable to decrease thermal capacitance and thermal resistance.

Claim 41 (Original) The packaged semiconductor device as recited in Claim 40, adapted for use in a surface mount assembly.

Claim 42 (Previously Presented) A packaged semiconductor device, comprising:  
a semiconductor die, a substrate and a plurality of leads, wherein at least one said lead has a shaped end configured to minimize parasitic capacitance over a predetermined frequency range;

the semiconductor die being disposed on the substrate;

a coupling means extending from the plurality of leads to the semiconductor die for providing low capacitance electrical connections which supports device functionality; and

an encapsulation material surrounding the semiconductor die, plurality of leads and coupling means, the encapsulation material making contact with the substrate operable to allow direct dissipation shunting to thermal ground, the encapsulation material having a consistent dielectric constant over the predetermined frequency range.

Claim 43 (Original) The packaged semiconductor device as recited in Claim 42, adapted for use in a surface mount assembly.

Claim 44 Canceled

Claim 45 Canceled

Claim 46 Canceled

Claim 47 Canceled

Claim 48 Canceled

Claim 49 Canceled

Claim 50 Canceled

Claim 51 (Withdrawn) A mount for a semiconductor device, comprising:

at least one lead portion having a top side, an opposing bottom side, a front edge, an opposing back edge, left edge and opposing right edge; and

the lead portion having dovetail or similar etched locking feature on a portion of its at least one of its front edge, left edge or right edge.

Claim 52 (Withdrawn) The mount of Claim 51, further comprising:

the at least one lead portion being part of a lead frame from which a plurality of semiconductor devices may be mounted; and

the back edge of the lead portion being part of the lead frame.

Claim 53 (Withdrawn) The mount of Claim 52, further comprising the at least one lead portion being adapted to be separated from the lead frame proximate the back edge.

Claim 54 (Withdrawn) The mount of Claim 51, wherein the dovetail or similar etched locking feature further comprises a substantially angled or curved plane along the front edge, from the bottom side to the top side of the at least one lead.

Claim 55 (Withdrawn) The mount of Claim 51, wherein the dovetail or similar etched locking feature is located on the front edge.

Claim 56 (Withdrawn) The mount of Claim 51, further comprising the edge having the dovetail or similar etched locking feature being functional to allow an encapsulant to couple to the top side, front edge, left edge and right edge of the at least one lead.

Claim 57 (Withdrawn) The mount of Claim 56, wherein the encapsulant comprises an epoxy.

Claim 58 (Withdrawn) The mount of claim 57, further comprising:

the epoxy locking on the at least one lead on the top side and three edges; and

the bottom side of the at least one lead remaining exposed.

Claim 59 (Withdrawn) The mount of Claim 55, further comprising:



an encapsulant enclosing a semiconductor die at the top side, front edge, left edge and right edge of the least one lead; and

the exposed bottom side of the at least one lead portion operable to shunt heat to thermal ground.

Claim 60 (Withdrawn) The mount of Claim 59, wherein thermal ground comprises a PCB.

Claim 61 (Withdrawn) A mounting for a plurality of semiconductor devices, comprising a lead frame having a plurality of leads; and

each of the plurality of leads having at least one edge with a dovetail or similar etched locking feature.

Claim 62 (Withdrawn) The mounting of Claim 61, wherein the lead frame comprises a thick lead frame material.

Claim 63 (Withdrawn) The mounting of Claim 61 wherein the lead frame material comprises copper.

Claim 64 (Withdrawn) The mounting of Claim 61, adapted for having disposed thereon a semiconductor die.

Claim 65 (Withdrawn) The mounting of Claim 61, being adapted for being encapsulated with an epoxy material.